

(b) Write the sequence of control steps required to execute the instruction Add R4, R5, R6 in the above drawn data path. 5

8. Write short notes on any two of the following : 5 x 2

(i) CD-ROM

(ii) Carry save addition

(iii) DMA.

Direct Memory Access
(without using CPU)

memory ↔ I/O device
under the control of a
DMA controller
Ex: Intel 8257, 8259

ADD R4, R5, R6

↓
add them
acc.

Q.6) size = 8KB

= (8 x 1024) bytes

1 block = 16 bytes

So, no. of blocks = $\frac{8KB}{16 \text{ bytes}}$

= $\frac{8 \times 1024}{16} = 512$

main memory = 64 MB
cache = 8KB of 512 blocks

MOV A, R6
ADD R5
ADD R4

COMPUTER SYSTEM ARCHITECTURE

Full Marks : 70

Time : 3 hours

Answer any six questions including

Q. No. 1 which is compulsory

The figures in the right-hand margin indicate marks

1. Answer the following questions :

2 x 10

(a) Size of PC in a microprocessor in 20 bits.

What will be size of the addressable memory space? 128 KB

(b) What is a program status word?

PSW - status flags & undefined bits

(c) What is the advantage of autoindexing?

(d) Differentiate between multiprocessor and multicomputer.

more than one CPU

$2^{20} \text{ bits} = 2^{20} \text{ bytes} = 2^7 \text{ bytes} = 2^7 \text{ bytes} = 128 \text{ KB}$

(Turn Over)

(e) Distinguish between spatial locality and temporal locality. (adjacent)

(f) How SRAM ^{Static RAM} does differ from that of DRAM?

(g) What is the difference between an arithmetic shift and a logical shift? ^{dynamic RAM}

(h) Give a reason for the use of guard bit in floating-point arithmetic.

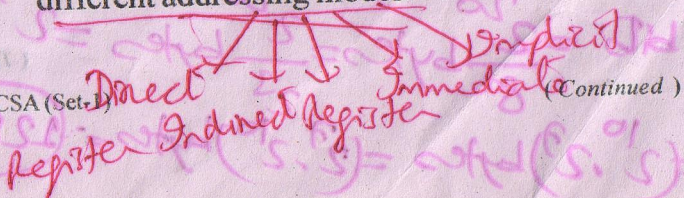
(i) List two major functions of an I/O module.

(j) What are the four essential elements of a number in floating-point number?

2. (a) Name the components of a digital computer. Explain the function of each component. ^{3.5 x 10³¹}

(b) What are the characteristics of a RISC instruction set architecture?

3. (a) List the relative merits and demerits of different addressing modes.



```
MVI C, 00H
LXI H, 2000H
MOV A, M
INX H
ADD M
JNC AHEAD
```

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INR C
AHEAD STA 2002H
(3)
MOV A, C
STA 2003H
HLT
```

(b) Write an assembly language program to add two 8-bit decimal number. 5

4. (a) Explain the set-associative cache mapping technique. 5

(b) A two-way set associative cache has blocks of 16 bytes and a total size of 8 KB. The 64 MB main memory is byte addressable. Show the format of main memory. 5

5. (a) Define virtual memory. Explain how a virtual address is translated into a physical address. 5

(b) Represent the number-0.5 in IEEE 64-bit floating-point format. 5

6. (a) Explain how an interrupt driven I/O is different from programmed controlled I/O? 5

(b) Explain lookahead carry addition with a suitable example. 5

7. (a) Draw a three-bus organization of data path inside a processor. 5